What is claimed is:

1. A method of performing a request from a central processing unit that uses memory-mapped input-output space, the method comprising:

converting a request directed to the input-output space of the central processing unit to a corresponding command that simulates an operation between components in a second processing domain;

executing the command in the second processing domain; and

accessing information according to the request in response to executing the command.

2. The method of claim 1 wherein the second processing domain comprises a multithreaded processing domain.

3. A method of writing information from a central processing unit that uses memory-mapped input-output space, the method comprising:

sending a request from the central processing unit to an address in the input-output space, wherein the address is associated with a destination in an bus interface unit;

converting the address and a command type associated with the request to a corresponding command having a format used

for communications between an engine in the bus interface unit and one or more micro-coded processing engines; and

executing the command in the engine in the bus interface unit; and

writing the information to the destination in the bus interface unit in response to executing the command.

4. The method of claim 3 including:

causing a control signal to be sent from the engine in the bus interface unit; and

promoting the information, in response to the control signal, onto a bus used for communications between the bus interface unit and the one or more micro-coded processing engines.

5. The method of claim 4 including giving the command a higher priority than commands from the one or more micro-coded processing engines.

6. A method of writing information from a central processing unit that uses memory-mapped input-output space, the method comprising:

sending a request from the central processing unit to an address in the input-output space, wherein the address is associated with a destination in a micro-coded processing engine;

converting the address and a command type associated with the request to a corresponding command in a format used for communications between an engine in a bus interface unit and the micro-coded processing engine;

executing the command in the engine in the bus interface unit; and

writing the information to the destination in the micro-coded processing engine in response to executing the command.

7. The method of claim 6 including:

causing a control signal to be asserted by the engine in the bus interface unit; and

promoting the information, in response to the control signal, onto a bus used for communications between the bus interface unit and the micro-coded processing engine.

8. The method of claim 7 including:

causing the engine in the bus interface unit to assert address signals on a bus used for communications between the bus interface unit and the micro-coded processing engine, wherein the asserted address signals enable the micro-coded processing engine to accept the information.

9. The method of claim 7 including giving the command a higher priority than commands from the micro-coded processing engine.

10. A method of providing information from a bus interface unit to a central processing unit that uses memory-mapped input-output space, the method comprising:

sending a request from the central processing unit to an address in the input-output space, wherein the address is associated with a location in the bus interface unit;

converting the address and a command type associated with the request to a corresponding command having a format used for communications between an engine in the bus interface unit and one or more micro-coded processing engines;

executing the command in the engine in the bus interface unit; and

providing the information to the central processing unit in response to executing the command.

11. The method of claim 10 including:

promoting the information from the location in the bus interface unit onto a first bus used for communications between the bus interface unit and the one or more micro-coded processing engines.

12. The method of claim 11 including:

causing a control signal to be asserted by the engine in the bus interface unit; and

promoting the information, in response to the control

signal, from the first bus to a second bus coupled to the central processing unit.

13. The method of claim 11 including giving the command a higher priority than commands from the one or more micro-coded processing engines.

14. A method of providing information from a micro-coded processing engine to a central processing unit that uses memory-mapped input-output space, the method comprising:

sending a request from the central processing unit to an address in the input-output space, wherein the address is associated with a location in the micro-coded processing engine;

converting the address and a command type associated with the request to a corresponding command having a format used for communications between an engine in a bus interface unit and the micro-coded processing engine;

executing the command in the engine in the bus interface unit; and

providing the information to the central processing unit in response to executing the command.

15. The method of claim 14 including:

promoting the information from the location in the micro-coded processing engine onto a first bus used for

communications between the bus interface unit and the micro-coded processing engine.

16. The method of claim 15 including:

causing a control signal to be asserted by the engine in the bus interface unit; and

promoting the information, in response to the control signal, from the first bus to a second bus coupled to the central processing unit.

17. The method of claim 15 including giving the command a higher priority than commands from the micro-coded processing engine.

18. A parallel hardware-based multithreaded processor comprising:

a central processing unit that coordinates system functions and that uses memory-mapped input-output space;

micro-coded processing engines that support multiple threads;

a bus interface unit;

a first bus coupled to the central processing unit; and

a second bus coupled to the micro-coded processing engines; and

a translator unit coupled between the first bus and the second bus to convert a request that is addressed to the

input-output space of the central processing unit to a corresponding command that simulates operations between the bus interface unit and the micro-coded processing units.

19. The processor of claim 18 including a command bus that couples the translator unit to the bus interface unit, wherein the bus interface unit includes a plurality of engines for causing information to be pushed or pulled onto the second bus in response to a command received from the translator unit via the command bus.

20. The processor of claim 19, wherein the bus interface unit includes a plurality of registers, and wherein information stored by a particular one of the registers is passed to the central processing unit via the second bus, the translation unit and the first bus as a result of the command being received and executed by one of the engines in the bus interface unit.

21. The processor of claim 19, wherein the bus interface unit includes a scratchpad, and wherein information stored by the scratchpad is passed to the central processing unit via the second bus, the translation unit and the first bus as a result of the command being received and executed by one of the engines in the bus interface unit.

22. The processor of claim 19, wherein the micro-engines include a plurality of registers, and wherein information stored by a particular one of the registers is passed to the central processing unit via the second bus, the translation unit and the first bus as a result of the command being received and executed by one of the engines in the bus interface unit.

23. The processor of claim 19, wherein the bus interface unit includes a plurality of registers, and wherein information addressed to the input-output space of the central processing unit is passed to a particular one of the registers via the translation unit and the second bus as a result of the command from the translation unit being received and executed by one of the engines in the bus interface unit.

24. The processor of claim 19, wherein the bus interface unit includes a scratchpad, and wherein information addressed to the input-output space of the central processing unit is written to the scratchpad via the translation unit and the second bus as a result of the command being received and executed by one of the engines in the bus interface unit.

25. The processor of claim 19, wherein the micro-engines include a plurality of registers, and wherein information addressed to the input-output space of the central processing

unit is written to a particular one of the registers via the translation unit and the second bus as a result of the command being received and executed by one of the engines in the bus interface unit.

26. The processor of claim 19 including a bus for sending control signals from the bus interface unit to the translation unit, wherein the translation unit includes a plurality of registers that respond to control signals from the engines in the bus interface unit to supply targeted information onto the second bus or to receive targeted information from the second bus.

27. An article comprising a computer-readable medium which stores computer-executable instructions for causing a computer system to:

convert a request addressed to input-output space of a central processing unit to a corresponding command that simulates an operation between components in a multithreaded processing domain;

execute the command in the multithreaded processing domain; and

cause information to be accessed according to the request in response to executing the command.